CLAIMS

What is claimed is:

1. A semiconductor memory device comprising an array (200) of memory cells arranged in rows and columns, wherein said array (200) of memory cells comprises:

a plurality of non-intersecting shallow trench isolation (STI) regions (650) isolating a plurality of said columns of memory cells;

a plurality of common source (Vss) lines coupled to a source column (260) arranged according to said columns that are coupled to a plurality of source regions in said array (200) of memory cells; and

an area (605) proximate to a lower portion of non-adjacent said STI regions implanted with n-type dopants for enhancing conductivity of said Vss lines.

2. The semiconductor memory device as recited in Claim 1 wherein said source column (260) is implanted with n-type dopants isolated between an adjoining pair of said plurality of non-intersecting STI regions (650).

3. The semiconductor memory device as recited in Claim 1 wherein said non-adjacent said STI regions (650) comprise alternating said STI regions.

4. The semiconductor memory device as recited in Claim 3 wherein said n-type dopants for enhancing conductivity of said Vss lines comprise an alternating Vss interconnection.

5. The semiconductor memory device as described in claim 1, wherein said n-type dopants are selected from the group consisting of antimony and arsenic.

6. The semiconductor memory device as described in claim 1, wherein said area (605) proximate to a lower portion of non-adjacent said STI regions (650) comprises a region beneath said STI region.

7. The semiconductor memory device as described in claim 1, wherein diffusion of said n-type dopants for enhancing conductivity of said Vss lines into a substrate further comprising said array (200) does not reach an adjacent said STI region (650).

8. The semiconductor memory device as described in claim 1, wherein said n-type dopants for enhancing conductivity of said Vss lines are implanted at low energy.

9. The semiconductor memory device as described in claim 1, wherein said n-type dopants for enhancing conductivity of said Vss lines are implanted at low dosage.

10. A non-volatile semiconductor memory device comprising an array (200) of memory cells arranged in rows and columns, wherein said array (200) of memory cells comprises:

a plurality of non-intersecting shallow trench isolation (STI) regions (650) isolating a plurality of said columns of memory cells;

a plurality of common source (Vss) lines coupled to a source column (260) arranged according to said columns that are coupled to a plurality of source regions in said array (200) of memory cells; and

an area (605) proximate to a lower portion of non-adjacent said STI regions (650) implanted with n-type dopants for enhancing conductivity of said Vss lines.

11. The non-volatile semiconductor memory device as recited in Claim 1 0wherein said source column is implanted with n-type dopants isolated between an adjoining pair of said plurality of non-intersecting STI regions.

12. The non-volatile semiconductor memory device as recited in Claim 10 wherein said non-adjacent said STI regions comprise alternating said STI regions.

13. The non-volatile semiconductor memory device as recited in Claim 10 wherein said n-type dopants for enhancing conductivity of said Vss lines comprise an alternating Vss interconnection.

14. The non-volatile semiconductor memory device as described in claim 10, wherein said n-type dopants are taken from a group consisting of antimony and arsenic.

15. The non-volatile semiconductor memory device as described in claim 10, wherein said area proximate to a lower portion of non-adjacent said STI regions comprises a region beneath said STI region.

16. The non-volatile semiconductor memory device as described in claim 10, wherein diffusion of said n-type dopants for enhancing conductivity of said Vss lines into a substrate further comprising said array does not reach an adjacent said STI region.

17. The non-volatile semiconductor memory device as described in claim 10, wherein said n-type dopants for enhancing conductivity of said Vss lines are implanted at low energy and low dosage.

18. A method of fabricating a semiconductor memory device comprising an array of memory cells arranged in rows and columns, wherein said array of memory cells has an alternating common source line (Vss) interconnection, comprising:

depositing nitride on a silicon substrate;

patterning said nitride to form a pattern for a plurality of shallow trench isolation (STI) regions;

etching said silicon to form said STI regions according to said pattern; and

implanting an n-type dopant in an area proximate to a lower portion of non-adjacent said STI regions.

19. The method as recited in Claim 18 further comprising forming an oxide liner on walls comprising said STI regions.

20. The method as recited in Claim 19 wherein said implanting is performed selectively prior to and after said forming an oxide liner.

21. The method as recited in Claim 18 wherein said n-type dopant comprises a material selected from the group consisting essentially of antimony and arsenic.

22. The method as recited in Claim 21 wherein said implanting is performed at a low energy and comprises a low dosage.